Fig. 1

Information symbols

g1

0   1   0

t

Fig.2a

g2

Sequence_I

t

Fig.2b

g3

Sequence_Q

t

Fig.2c

g4

Sequence_Q after baseband filtering

t

Fig.2d

g5

Sequence_I after baseband filtering

t

Fig.2e

g6

Chirp signal

t

Fig.2f

Fig.2 a - f

Chirp Generation

CML Logic

TX 2441.75MHz
RX 2591.75MHz → 1/2 > 1/5 → to LO Adjust

TX 122.0875MHz ← 1/2 < TX 244.175MHz

4.Order Butterworth 33MHz , 3 Poles active 1Pole passive, Frequency Adjustment by switched cap, integrated 6Bit DAC, 4+2 Segmentation

COS[LO]

SEQ → 6 → ROM 64x32 → 32 → MUX → 16 → MAP → 6 → DAC LPF → ⊗ → I Path

→ 8 → DAC LPF → ⊗ → Q Path

→ + → to PAC

MD[3:0] 4

SIN[LO]

COUNT SEQ 60->0->0->60

Chirp ROM stores 244 samples of an upchirp

122MHz/ 244MHz

IQ ROM to IQ DAC Mapping Definition

MD[3]	MD[2]	MD[1]	MD[0]	IDAC	QDAC	Description
			Basic Modes			
0	0	0	0	IROM	QROM	Upchirp
0	1	0	0	IROM	-QROM	Downchirp
1	0	x	x	IROM	0	Upchirp+Downchirp
1	1	x	x	0	QROM	Upchirp-Downchirp
			QPSK Up Modes			
0	0	0	0	IROM	QROM	0
0	0	0	1	QROM	-IROM	Pi/2
0	0	1	0	-IROM	-QROM	Pi
0	0	1	1	-QROM	IROM	3Pi/2
			QPSK Down Modes			
0	1	0	0	IROM	-QROM	0
0	1	0	1	QROM	IROM	Pi/2
0	1	1	0	-IROM	QROM	Pi
0	1	1	1	-QROM	-IROM	3Pi/2
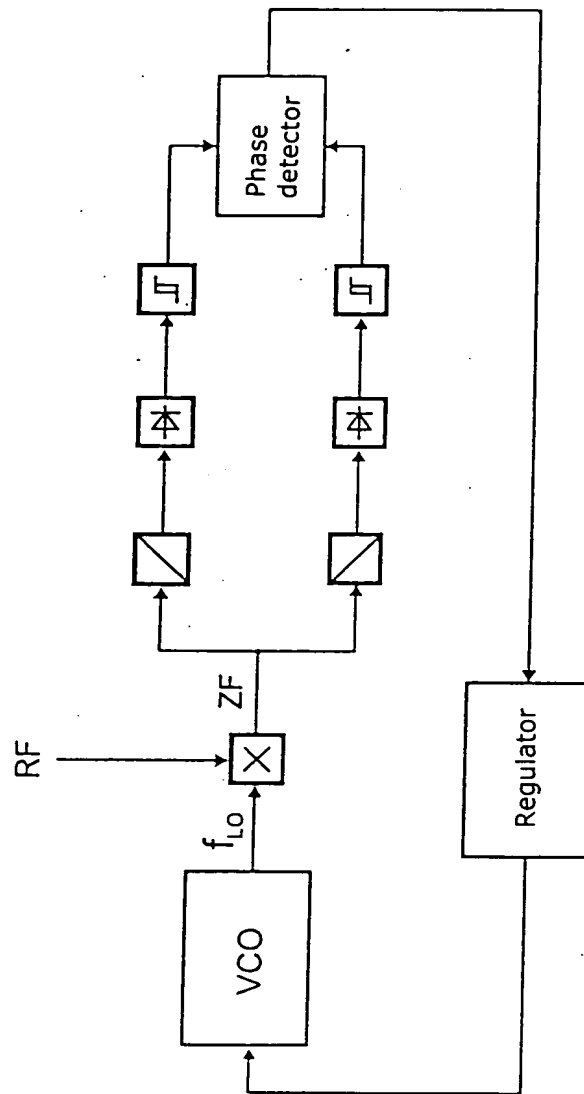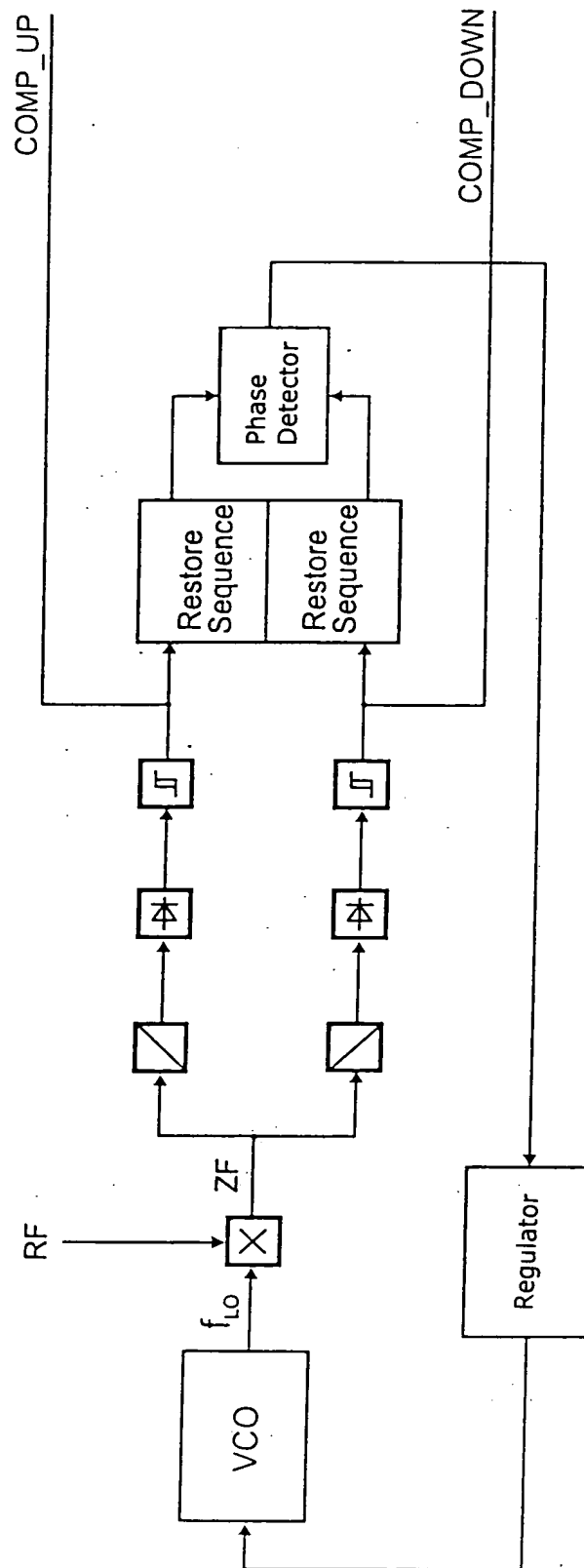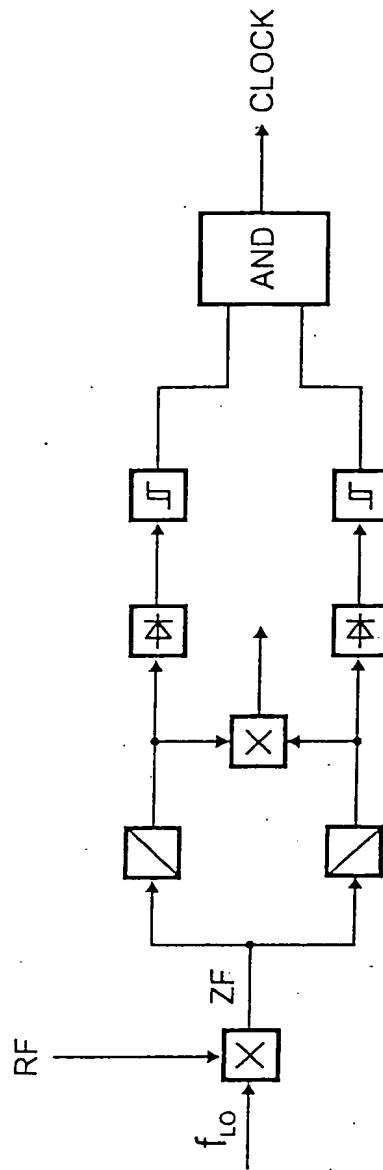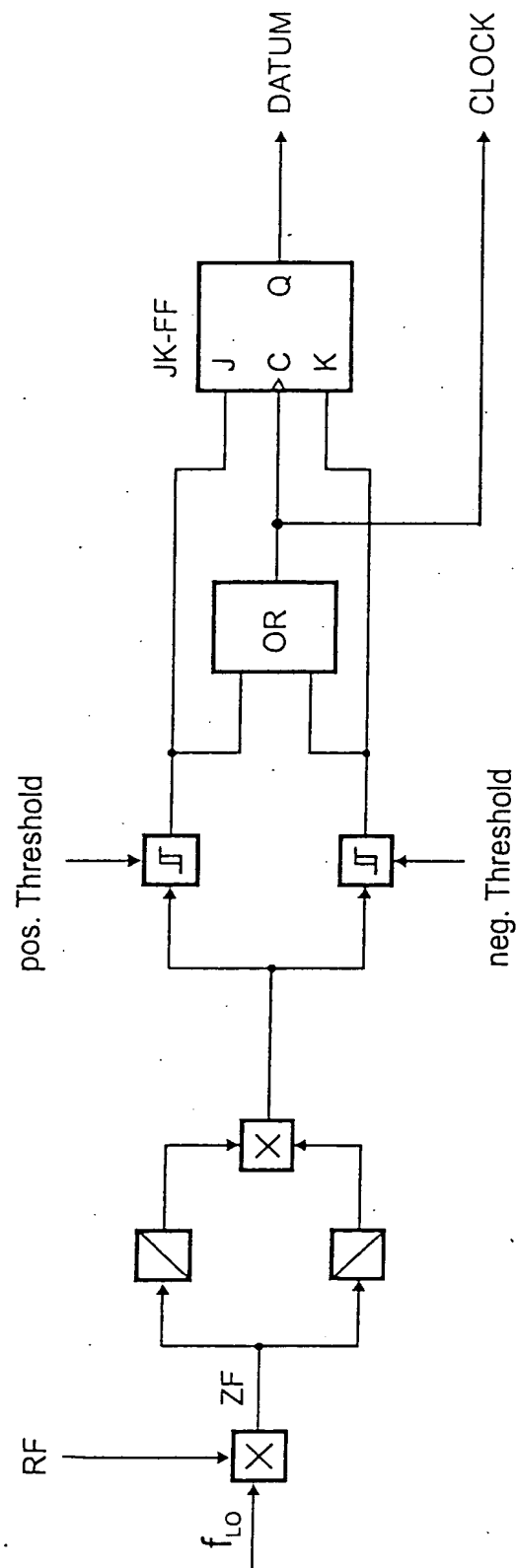
Fig. 2g

Fig. 3

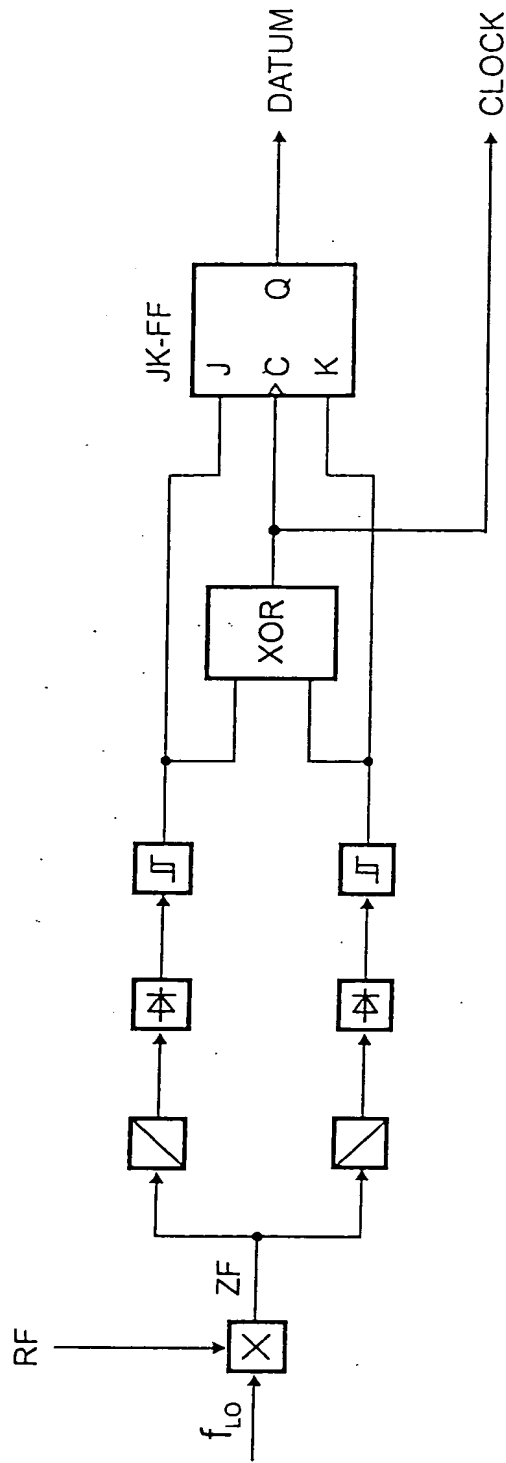COMP_UP
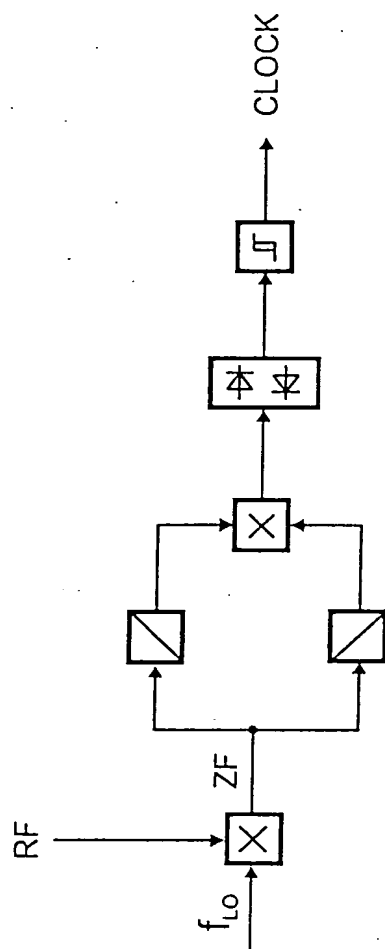
COMP_DOWN

Phase
Detector

Restore
Sequence

Restore
Sequence

RF

ZF

f_{LO}

VCO

Regulator

Fig. 4

Fig. 5

Fig. 6

Fig. 7

DATUM

CLOCK

JK-FF

J

C

K

Q

OR

pos. Threshold

neg. Threshold

RF

f_{LO}

ZF

Fig. 8

CLOCK_G

g10

CLOCK g8

GATE Signal g9

Time control

Fig. 9

Fig. 10

CLOCK_G

g10

AND

MONOFLOP

g8

g9

CLOCK

GATE-Signal

Fig. 11

COMP_UP

COMP_DOWN

Average Detector

Peak Detector

Average Detector

Peak Detector

RF

f_{LO}

ZF

Fig. 12

COMP_UP

COMP_DOWN

U_min

U_min

Average Detector

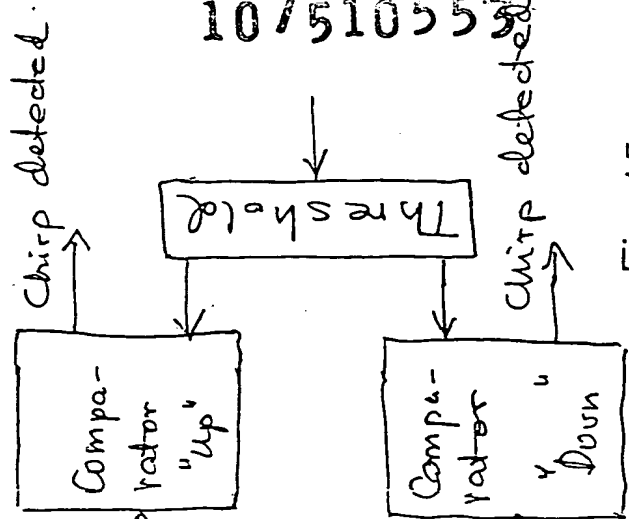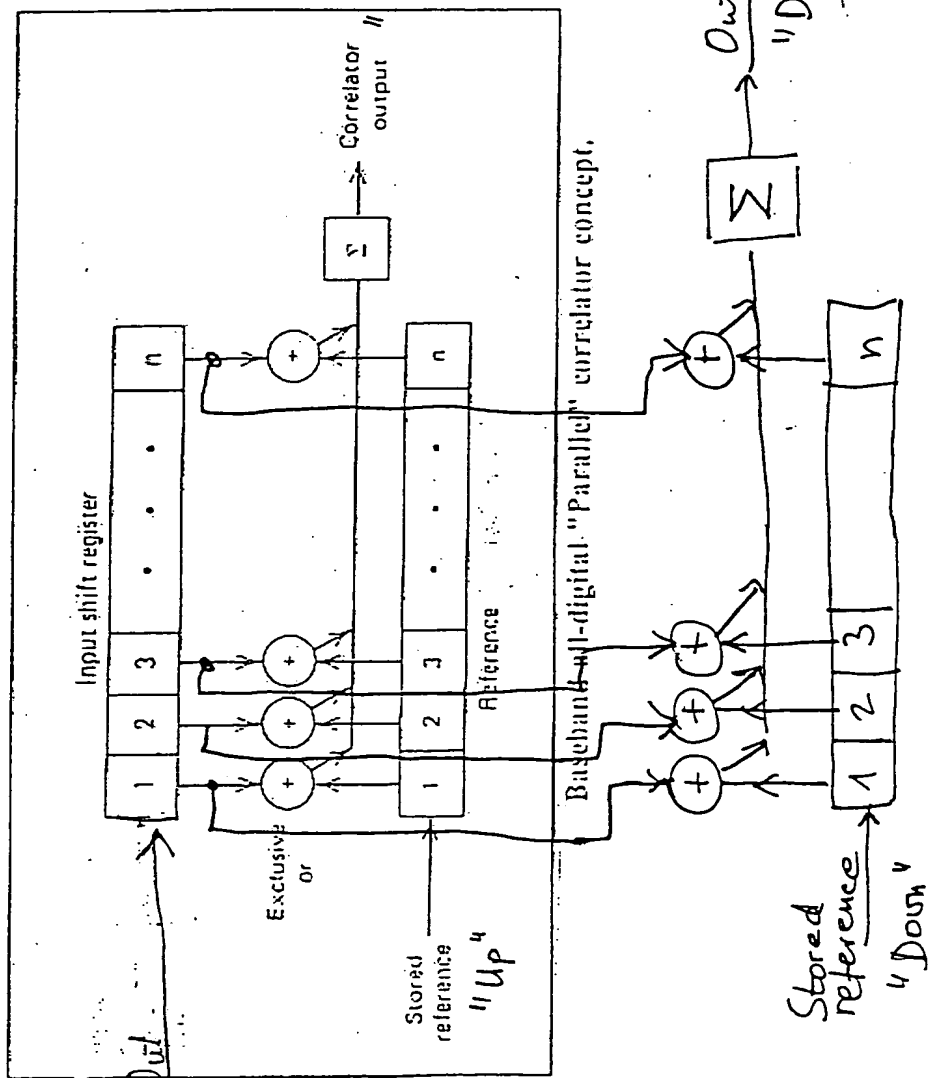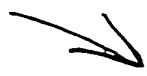Peak Detector

Average Detector

Peak Detector

RF

ZF

f_{LO}
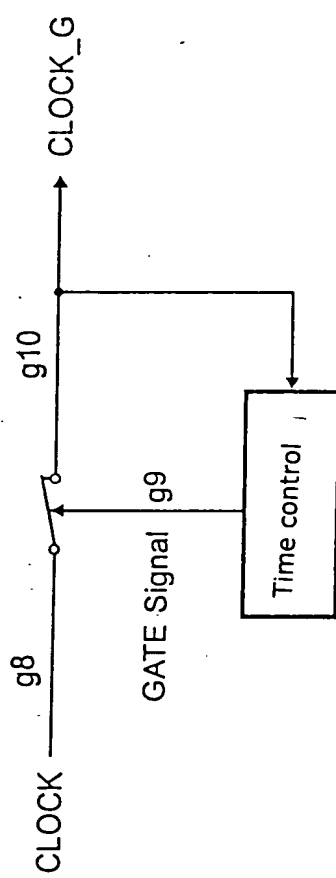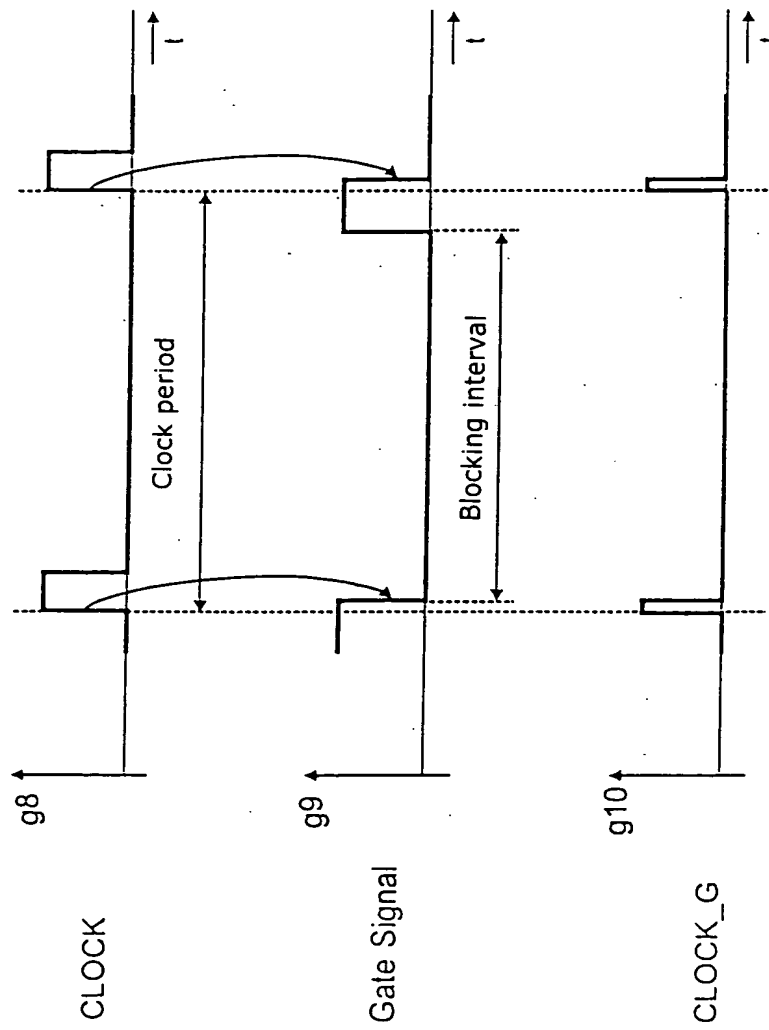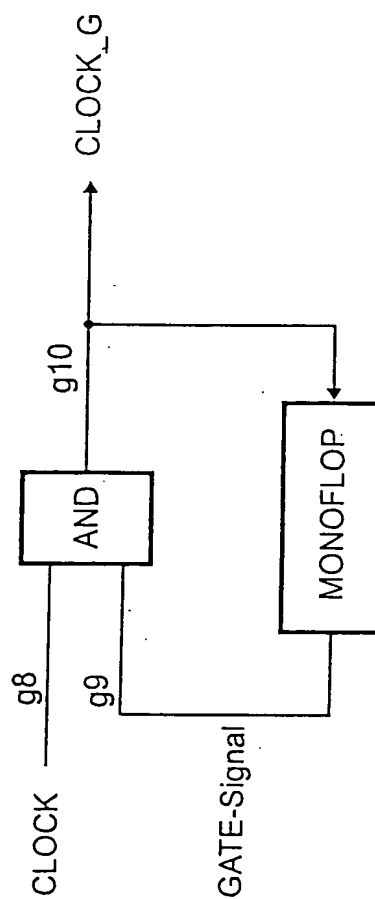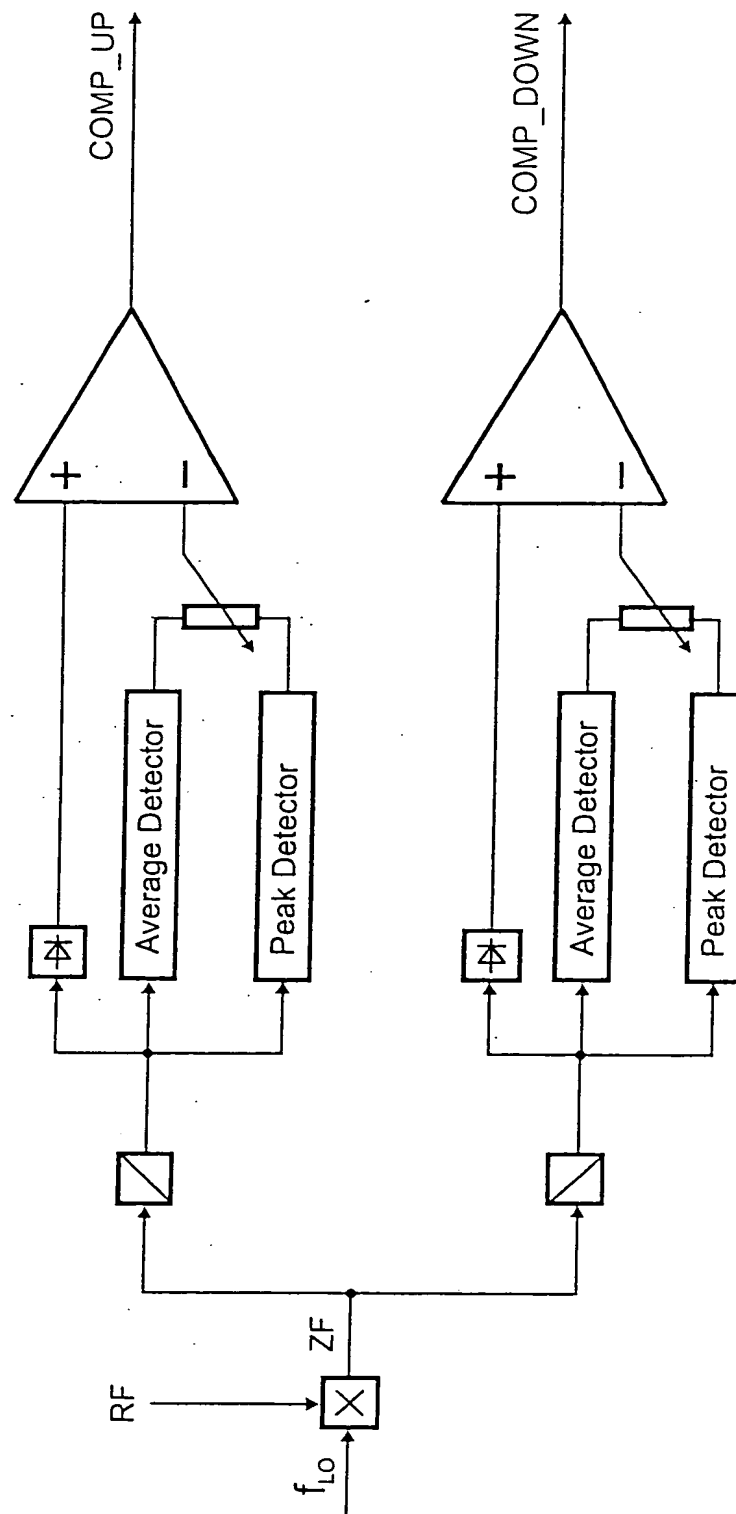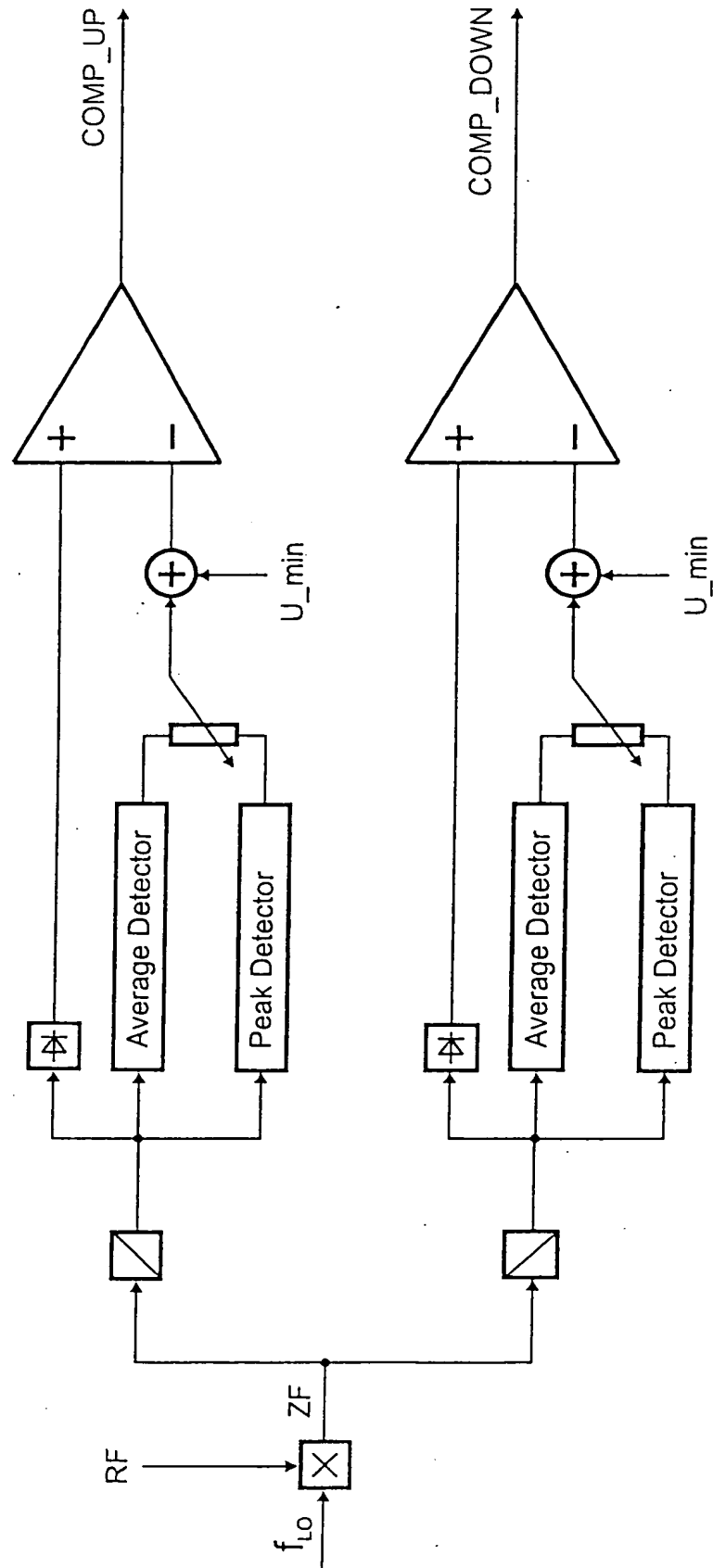
Fig. 13
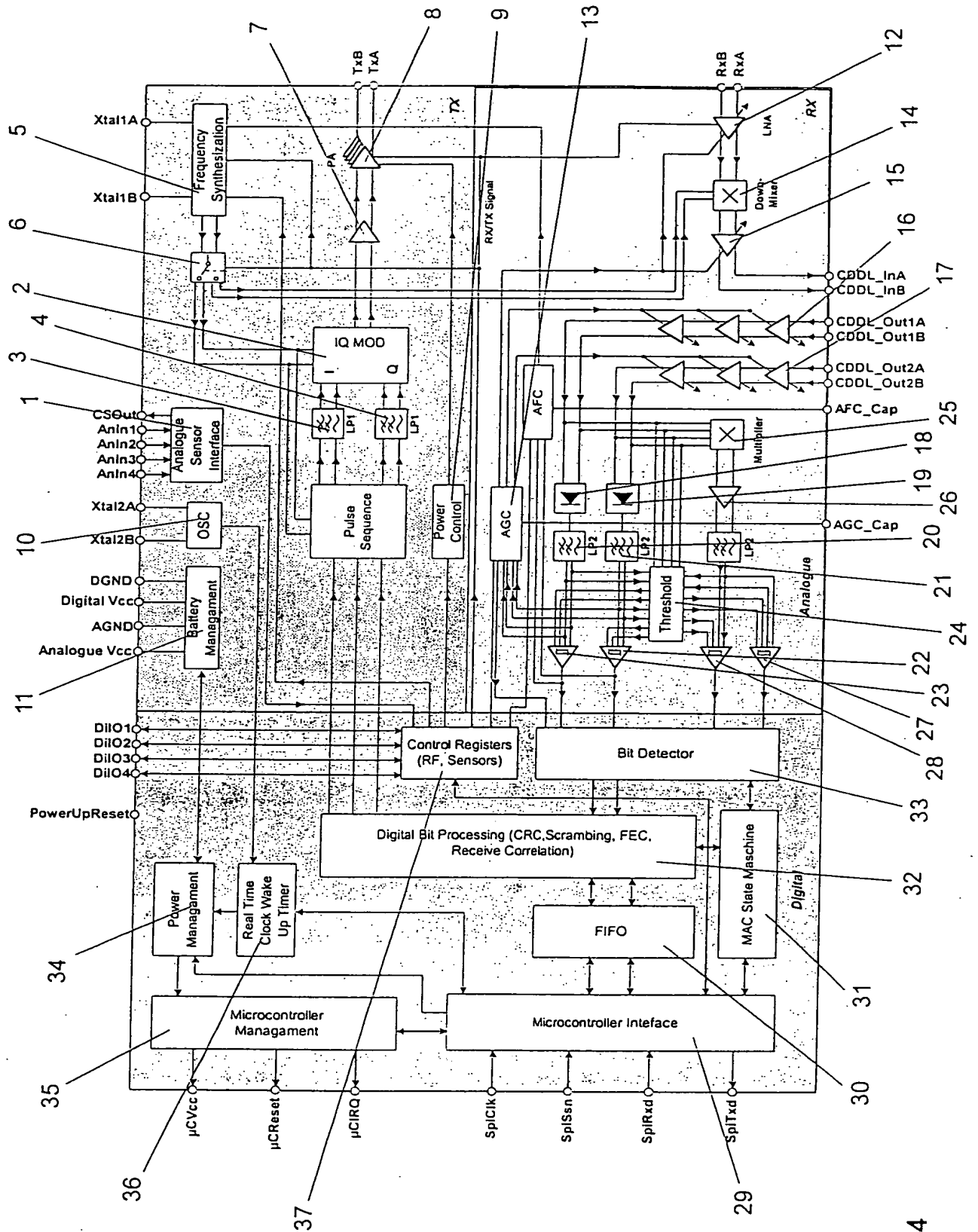
Fig. 14

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Fig. 15

DDDL

Differential Comparator

A > B then Out = 1
otherwise Out = 0

Baseband full-digital "Parallel" correlator concept.

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Fig. 16